REMARKS

Claims 11-21 are pending in this application, all of which have been added. Claims 1-10 have been canceled.

The recitation "extending over a semiconductor substrate throughout" in the respective second line in newly-added claims 11 and 16 is supported by cross-sections of Figs. 2 and 4 in which ground plate 3, which is not a line or strip, extends entirely over a semiconductor substrate and under pad region and wiring region throughout.

Claims 1-8 and 10 stand rejected under 35 USC §103(a) as unpatentable over U.S. Patent 6,162,686 to Huang et al. (hereinafter "**Huang et al.**) in view of U.S. Patent 5,427,979 to Chang (hereinafter "**Chang**").

Applicants respectfully traverse this rejection.

As noted in the Preliminary Amendment filed April 7, 2003, **Huang et al.** discloses a method of forming a grooved fuse (plug fuse) in the same step that via plugs are formed in the guard ring area 14 and in product device areas. The groove is provided to alleviate the stress which is applied to the pad and would propagate therefrom to the line conductor during bonding of the wire to the pad. Key guard rings are formed around the plug guise. A semiconductor structure is provided having a fuse area, a guard ring area surrounding the fuse area, and a device area. First and second conductive strips are formed. First and second insulating layers are formed over the first and second conductive strips. Plug contacts and fuse plugs are formed through the first and second insulating layers to the first and second conductive strips. A third insulating layer is formed over the second insulating layer. Metal lines are formed over the third insulating

layer in the device area. A fuse via opening is formed in the third insulating layer. A plug fuse is formed in the fuse via opening. A fourth insulating layer is formed over the plug fuse and the third insulating layer. A fuse opening is formed at least partially through the fourth insulating layer over the fuse area.

Fig. 5 shows pads 72 provided on the upper most interlayer insulation film 66, where the pads 72 are separated by the groove. **Huang et al.** fails to show a line conductor, distinct from the pad, on an upper surface of the upper most interlayer insulation film 66. Although third plug ring 68 may be considered a line conductor, it is arranged within the upper most interlayer insulation film 66, not on the upper surface, as in the present invention.

The Examiner continues to urge that the cross-sections 72 in Fig. 5 of **Huang et al.** are a line conductor and a pad, respectively. However, each of the cross-sections 72 is a portion of a ring-shaped pattern and is the upper-most metal layer forming guard ring 74 as shown in Fig. 6 of **Huang et al**. Thus, the cross-sections 72 in Fig. 5 of **Huang et al.** are not separated each other but instead form a single body.

If the cross-section 72 in the right-hand side is a line conductor, the cross-section 72 in the left-hand side is also a line conductor and cannot be a pad.

Fuse window 84 in **Huang et al.**, which is regarded by the Examiner as corresponding to the groove in the present invention, is formed in the insulating layer in the area inside the ring-shaped pattern. Hence, the fuse window 84 should be a groove formed between line conductors or between pads. The fuse window 84 is provided for facilitating the cutting of plug fuse 58B by irradiation of a laser beam applied thereto through fuse window 84. Thus, such a groove as fuse

window 84 does not teach the effect of the groove in the present invention in which the groove alleviates the stress propagating from the pad to the line conductor, when it is applied to the pad during the wire bonding to the pad.

The Examiner has also admitted that **Huang et al.** does not disclose that pad 72 is on the upper surface of insulating film 76, but has cited **Chang** for teaching this feature.

Applicants respectfully disagree. **Chang** discloses a method for making a multi-level antifuse structure, in which a third conductive layer 48 is disclosed.

Column 5, lines 15-20 disclose:

> The third conductive layer 48 is, again, preferably a sandwich of TiW, Al and TiW. The third conductive layer 48 is preferably patterned by conventional photolithography techniques to form conductive lines which couple the antifuse structure 28 of the present invention to other circuit elements of the integrated circuit.

Thus, although **Chang** can be said to teach conductive lines on the upper structure of the antifuse structure, there is no suggestion of a pad being provided on the upper surface of a most upper one of the interlayer insulation film, as recited in claim 1 of the instant application.

Chang discloses an "antifuse structure", and not a "fuse structure". Antifuse layers 36 and 42 in Fig. 2 of **Chang** are formed of amorphous silicon (A-Si) and have high resistance (1 giga-ohms, for example), and conductive paths of low resistance such as 20 to 100 ohms are established for a current flowing in vertical direction (in the direction along thickness of the layers). Thus, it is apparent that the technology of **Chang** is different from that of **Huang et al.**, and only the term "fuse" is common between **Chang** and **Huang et al**.

Chang discloses third conductive layer 48 formed on the top surface of an insulating layer, which is no more than a wiring means for a supplying currents to antifuse layers 36 and 42 through conductive via 46 and is electrically connected to another peripheral circuit. (See the plan view of Fig. 3).

On the other hand, the fourth metal ring 72 in **Huang et al.**, which is a layer forming guard ring 74, is electrically isolated from surrounding and has a ring shape. Therefore, the fourth metal ring 72 in **Huang et al.** differs from third conductive layer 48 in **Chang** in terms of its shape and object.

Thus, there would be no motivation to combine the third conductive layer 48 in **Chang** and the fourth metal ring 72 in **Huang et al**.

The recitation that each of the line conductors forms a strip-line with the ground plate in claim 11 is supported by the description with reference to Fig. 1, in page 1 of the specification, although this refers to prior art, because Fig. 2, showing the present invention, is the same as Fig. 1 except groove 7 which is a distinction between the prior art and the present invention.

The ground plate is supplied with a constant potential which is, typically, the ground (earth) potential, as described in page 3 of the specification.

Huang et al. relates to a fuse structure and differs greatly from a semiconductor device having micro-strip lines, as disclosed in the present invention.

The conductive strips 20A in **Huang et al.** merely constitute a wiring in a fuse and not a ground plate for micro-strip lines. **Huang et al.** does not teach, mention or suggest that the

conductive strips 20A acts as a ground plate for forming a micro-strip line.

Accordingly, claims 11-21 have been added which recite that each of said line conductors form a micro-strip line in conjunction with the ground plate.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claim 9 stands rejected under 35 USC §103(a) as unpatentable over **Huang et al.** in view of **Chang** and further in view of U.S. Patent 4,417,701 to Moritz (hereinafter "**Moritz**").

Applicants respectfully traverse this rejection.

The Examiner has cited **Moritz** for teaching the insulating film being made of polyamide or benzocyclobutene.

Moritz, like the other cited references, fails to teach, mention or suggest the other limitations in newly-added claims 11-21.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, newly-added claims 11-21, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

William L. Brooks
Attorney for Applicant
Reg. No. 34,129

WLB/mla
Atty. Docket No. **020129**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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